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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/649,819	08/28/2003	Eliezer Magal	2896/6	5986

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EXAMINER	
CHO, JAMES HYONCHOL	

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 01/11/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/649,819	MAGAL ET AL.	
	Examiner	Art Unit	
	James Cho	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 August 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-41* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,14-21,23-25,34 and 37* is/are rejected.

7)☒ Claim(s) *4-13, 22, 26-33, 35-36, and 38-41* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date ~~8-28-2003~~. 7-1-04
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-3, 14-21, 23-25, 34, and 37 are rejected under 35 U.S.C. 102(b) as being anticipated by Mughal et al. (US PAT No. 6,411,122).

Regarding claims 1 and 37, Fig. 1 of Mughal et al. teaches a system or a method for transmitting data (co. 2, lines 31-38) , the system comprising: at least one bus data line (16), at least one transmitter (12), each transmitter including: for each of the at least one bus data line, a respective open-driver bus data line driver (22), each the open-driver bus data line driver drivingly connected to a corresponding the bus data line (the system 10 includes devices 12, 14 communicating via one or more buses 16, col. 2, lines 31-38).

Regarding claim 2, Fig. 1 of Mughal et al. teaches the system of claim 1 where the transmitter further includes at least one transmit data line (line driving 22) for driving a respective the open-driver bus data line driver (22).

Regarding claim 3, Fig. 1 of Mughal et al. teaches the system of claim 2 where the transmitter further includes at least one active-pullup driver (Rtt1; col. 3, lines 44-49) drivingly connected to a respective the open-driver bus data line driver.

Regarding claim 14, Fig. 1 of Mughal et al. teaches the system of claim 1, further comprising a data-sense line (line connected to 36 in Fig. 2) operative to conduct a data-sense signal (the data-sense signal comprising of Data and EN signals).

Regarding claim 15, Figs. 1 and 2 of Mughal et al. teaches the system of claim 14, where the data-sense signal has a driven state (driving 36 is Fig. 2; col. 4, lines 18-57) and where each the transmitter further includes an open-driver data-sense signal line driver (36) operative to drive the data-sense signal line to the data-sense signal's driven state when the transmitter is transmitting data (transmit mode; col. 4, lines 24-49).

Regarding claim 16, Figs. 1 and 2 of Mughal et al. teaches the system of claim 15 where the open-driver data-sense signal line drivers of the at least one transmitter are connected in a wired-and configuration (36 in Fig. 2 coupled to Rtt and the node 18 in a wired-and configuration).

Regarding claim 17, Figs. 1 and 2 of Mughal et al. teaches the system of claim 14, further comprising a conductor at a high logic level (conductor coupled to Vtt in Fig.

2), and a resistor (Rtt1), the resistor being connected between the conductor (conductor coupled to Vtt) and the data-sense signal line (lines connected to 36).

Regarding claim 18, Fig. 1 of Mughal et al. teaches the system of claim 1, further comprising a conductor at a high logic level (conductor coupled to Vtt in Fig. 2), and a resistor (Rtt1 in Fig. 2), the resistor being connected between the conductor (conductor coupled to Vtt) and one the bus data line (the node 18 connected to the bus 16 in Fig. 1).

Regarding claim 19, Fig. 1 of Mughal et al. teaches the system of claim 1, further comprising a clock signal line (line receiving Clock in Fig. 1), operative to transmit a clock signal (Clock) to the transmitter (12).

Regarding claim 20, Fig. 1 of Mughal et al. teaches the system of claim 1, further comprising a receiver operative to receive data from the bus data lines (14).

Regarding claim 21, Fig. 1 of Mughal et al. teaches the system of claim 20, further comprising a clock signal line (line receiving Clock in Fig. 1), operative to transmit a clock signal (Clock) to the transmitter (12).

Regarding claim 23, Fig. 1 of Mughal et al. teaches the system of claim 1 where corresponding the open-driver bus data line drivers connected to a corresponding the

bus data line are connected in a wired-and configuration (22 and 16 are connected in a wired-and configuration).

Regarding claim 24, Fig. 1 of Mughal et al. teaches a system to connect a device (14) to a bus (16), the device having a transmitter (32, 30, 34, 22) and a receiver (26), the bus having a plurality of bus data lines (col. 2, lines 32-38), the bus being operative to be connected to other transmitters and to other receivers (24, 28), the system comprising for each of the bus data lines, a respective open-driver bus data line driver (22) suitable to be drivingly connected to the each bus data lines.

Regarding claim 25, Fig. 1 of Mughal et al. teaches the system of claim 24, further comprising at least one transmit data line (line connected to base of 22 accepts Data from 30) operative to accept data from the transmitter (32, 30) of the device and to drive a respective the open-driver bus data line driver (22).

Regarding claim 34, Fig. 1 of Mughal et al. teaches the system of claim 24, further comprising a conductor at a high logic level (conductor coupled to Vtt) and a resistor (Rtt), the resistor being connected between the conductor and one bus data line, the conductor and the resistor operative to cause the one bus data line to be at a high logic level when all the bus data line drivers connected to the one bus data line are in a high-impedance state (when all 22 and 24 are turned off, i.e. high impedance state, the pull-up resistor Rtt pulls up the data line 16 to a logic high Vtt).

Allowable Subject Matter

Claims 4-13, 22, 26-33, 35-36, and 38-41 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: Although Mughal et al. teaches an open-drain bus architecture system, one of ordinary skill in the art would not have been motivated to modify the teaching of Mughal et al. to further includes, among other things, the specific of a collision-detection mechanism detecting a data difference between one of the transmission data line and a corresponding bus data line, a data-valid signal line operative to transmit a data-valid signal and each of the open-driver bus data line driver of the transmitter to be in a high-impedance state when the data-valid signal is in an inactive state, as set forth in the claims.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

McCalmont (US PAT No. 6,822,480) discloses a bi-directional bus level translator.

Kamiya (US PAT No. 6,211,694) discloses a bus driver having noise removing circuit.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to James Cho whose telephone number is 571-272-1802. The examiner can normally be reached on M-F 6:30 AM - 3:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mike Tokar can be reached on 571-272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

James H. Cho
Primary Examiner
Art Unit 2819

Date: 12-30-2004